DETAILED ACTION

Response to Amendment

1. In view of applicant's amendment filed on 1/ 27/10, the status of the application is still pending with respect to claims 1-16 and 18-35.

Response to Arguments

2. Applicant's arguments filed on 1/27/10 have been fully considered but they are not persuasive.

Regarding claims 1, 2, 9, 30 and 31, the applicant argues that the cited art does not teach address translation without buffering a packet or at wire speed.

The examiner maintains that the claimed limitations interpreted within its broadest sense is taught by the cited references, wherein the combination of Latif and Ibrahim shows an address translation (Latif: Col 11 lines 15-30, IP address to FC address equivalent to virtualizing and Ibrahim: Col 4 lines 59-63), wherein, Latif makes no mention of a buffer, which implies a bufferless system. Despite the applicants arguments on page of the applicants remarks, the combined teachings of Latif and Ibrahim, **do not show a buffer within the switch of Latif or the controller of Ibrahim**. It is clear to one skilled in the art that the claimed "without buffering" requires the absence of a buffer. Thus the exclusion of a buffer in the combined teachings of Latif and Ibrahim make it clear that these devices are operating without buffering.

The applicant also argued that virtualizing does not occur at wire speed as indicated on pages 5-6 of the applicant’s remarks. The examiner maintains that the

claimed limitations interpreted within its broadest sense is taught by the combined teachings of Latif and Ibrahim, wherein Ibrahim (US 7,330,892) incorporates by reference , provisional application No. 60317817 page 9, 5.1.2 which specifically states

"The Network Processor has several microprocessors and one of them, also known as ***PICO processor****, can run several user defined threads coded in PICO language. The CVSS system would heavily depend on* ***PICO*** *processing to do the I/O processing at wire speed.* ***The I/O processing here means look-ups and mapping of Virtual LUNs/volumes to physical target ports.***

The PICO processing within an NP works as an intelligent routing and forwarding engine. The subsystem also known as ***PICO Command Router (PCR), does not buffer any data****. However, it does send multiple copies of data to different ports by using NP's HW features without duplicating it in the memory. In a normal system, during the runtime, an I/O request/response would be received by the NP and processed by the PICO subsystem. The PICO subsystem consists of 32 independent threads running at 133 MHz. The received frame is further interrogated by one of the threads to understand the request type and its mapping to the target port. The mapping, which depends on the I/O request (Read/Write/Others), length (block count), block address, and source/destination address, is pre-calculated in a table during the startup and the configuration of the NP. In the case where NP is unable to map a particular request, it further routes it to the next layer and that is CPU Command Router (CCR)."*

Therefore Ibrahim shows a PICO processor for performing I/O processing such as mapping addresses, at wire speed and without buffering data.

Regarding claims 30, 31 and 32, these claims are argued for the same reasoning as depicted above, so are therefore addressed above.

Regarding claims 3-8, 10-16, 18, 24-29 and 32-35, these claims are argued based on their dependency on the claims that precede, so are therefore addressed above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 9, 30, 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Latif et al. (US 6400730) in view of Ibrahim (US 7330892)

Regarding Claim 1, Latif discloses receiving at a first port **(fig 5, notice ports/interfaces in fig 5, where 270-5 includes an IP port interface)** of the switch **(fig 5, notice switch fabric)** a packet **(Col 2 lines 55-60 describes receiving a packet)** that specifies as a virtual storage target **(Col 11 lines 50-55, where the destination IP address is equivalent to the address of a virtual target)** provisioned on a physical storage target **(Col 11 lines 53-63, where the destination fibre channel address is equivalent to the address of the physical target, and is based/provisioned on the IP/virtual address, i.e. Col 5 lines 50-56, notice storage targets).**

sending at a second port **(fig5, notice FC interface equivalent to second port, and Col 2 lines 65-Col 3 line 5, data is routed to a second port)** of the switch **(fig 5, see switch fabric)** the packet to said physical storage target **(Col 3 lines 1-5, packet is transmitted to a second network device coupled to the second port).**

Wherein said sending comprises virtualizing said packet **(Col 11 lines 15-30, where address translation from an IP address to a FC address is equivalent to virtualizing)** by translating a first address **(Col 11 lines 15-30, where an IP address is**

equivalent to a first address of a virtual storage target) of said virtual storage target **(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target)** to a second address **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target)** of said physical storage target (**Col 3 lines 1-5, packet is transmitted to a second network device coupled to the second port, i.e. Col 5 lines 50-56, notice storage targets)**

Latif makes no mention of buffering in the switch shown in fig 5 or the port shown in fig 15.

Latif does not specifically disclose without buffering.

Ibrahim discloses without buffering the packet **(Col 4 lines 59-63 shows that the mappings of the virtual to the physical are performed, and data transfer is performed between the host and the storage device at wire speed, i.e. notice fig 3, where the elements within 302, have no need for a buffer, i.e. notice provisional application no. 60/317,817 page 9, 5.1.2, incorporated by reference, for showing mapping from virtual to physical at wirespeed and without buffering).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the switch apparatus of Latif, as taught by Ibrahim, since stated in Col 1 lines 60-65, that such a modification will overcome the effects of traffic on the network being slowed down and the overall throughput and latency deleteriously being reduced.

<u>Regarding claim 2,</u> Latif does not specifically disclose said virtualizing occurs at wire speed.

Ibrahim discloses said virtualizing occurs at wire speed **(Col 3 lines 15-20 shows wire speed, i.e. notice provisional application no. 60/317,817 page 9, 5.1.2, incorporated by reference, for showing mapping from virtual to physical at wirespeed and without buffering).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the switch apparatus of Latif, as taught by Ibrahim, since stated in Col 1 lines 60-65, that such a modification will overcome the effects of traffic on the network being slowed down and the overall throughput and latency deleteriously being reduced.

<u>Regarding Claim 9,</u> Latif discloses receiving at a first port **(fig 5, notice ports/interfaces in fig 5, where 270-5 includes an IP port interface)** of the switch **(fig 5, notice switch fabric)** a packet **(Col 2 lines 55-60 describes receiving a packet)** that specifies as a virtual storage target **(Col 11 lines 50-55, where the destination IP address is equivalent to the address of a virtual target)** provisioned on a physical storage target **(Col 11 lines 53-63, where the destination fibre channel address is equivalent to the address of the physical target, and is based/provisioned on the IP/virtual address, i.e. Col 5 lines 50-56, notice storage targets).**

sending at a second port **(fig5, notice FC interface equivalent to second port, and Col 2 lines 65-Col 3 line 5, data is routed to a second port)** of the switch **(fig 5, see switch fabric)** the packet to said physical storage target **(Col 3 lines 1-5, packet is transmitted to a second network device coupled to the second port).**

Wherein said sending comprises virtualizing said packet **(Col 11 lines 15-30, where address translation from an IP address to a FC address is equivalent to virtualizing)** by translating a first address **(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target)** of said virtual storage target **(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target)** to a second address **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target)** of said physical storage target (**Col 3 lines 1-5, packet is transmitted to a second network device coupled to the second port, i.e. Col 5 lines 50-56, notice storage targets)**

Latif makes no mention of buffering in the switch shown in fig 5 or the port shown in fig 15.

Latif does not specifically disclose at wire speed.

Ibrahim discloses at wire speed **(Col 4 lines 59-63 shows that the mappings of the virtual to the physical are performed, and data transfer is performed between the host and the storage device at wire speed, i.e. notice fig 3, where the elements within 302, have no need for a buffer, i.e. notice provisional application no. 60/317,817 page 9, 5.1.2, incorporated by reference, for showing mapping from virtual to physical at wirespeed and without buffering).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the switch apparatus of Latif, as taught by Ibrahim, since stated in Col 1 lines 60-65, that such a modification will overcome the effects of traffic on the

network being slowed down and the overall throughput and latency deleteriously being reduced.

<u>**Regarding claim 30,**</u> Latif discloses a port **(fig 5, notice ports/interfaces in fig 5, where 270-5 includes an IP port interface)**

Wherein said sending comprises virtualizing said packet **(Col 11 lines 15-30, where address translation from an IP address to a FC address is equivalent to virtualizing)** by translating a first address **(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target)** of said virtual storage target **(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target)** to a second address **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target)** of said physical storage target (**Col 3 lines 1-5, packet is transmitted to a second network device coupled to the second port, i.e. Col 5 lines 50-56, notice storage targets)**

Latif makes no mention of buffering in the switch shown in fig 5 or the port shown in fig 15.

Latif does not specifically disclose at wire speed.

Ibrahim discloses at wire speed **(Col 4 lines 59-63 shows that the mappings of the virtual to the physical are performed, and data transfer is performed between the host and the storage device at wire speed, i.e. notice fig 3, where the elements within 302, have no need for a buffer, i.e. notice provisional application no. 60/317,817 page 9, 5.1.2, incorporated by reference, for showing mapping from virtual to physical at wirespeed and without buffering).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the switch apparatus of Latif, as taught by Ibrahim, since stated in Col 1 lines 60-65, that such a modification will overcome the effects of traffic on the network being slowed down and the overall throughput and latency deleteriously being reduced.

Regarding claim 31, Latif discloses a plurality of ports **(fig 5, notice ports/interfaces in fig 5, where 270-5 includes an IP port interface)**

A plurality of processor units (see fig 15 for plurality of processor units in the ports) wherein each processor unit is associated with at least one respective port (fig 15 shows structure of ports)

Wherein said sending comprises virtualizing said packet **(Col 11 lines 15-30, where address translation from an IP address to a FC address is equivalent to virtualizing)** by translating a first address **(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target)** of said virtual storage target **(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target)** to a second address **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target)** of said physical storage target (**Col 3 lines 1-5, packet is transmitted to a second network device coupled to the second port, i.e. Col 5 lines 50-56, notice storage targets)**

Wherein the virtualization unit (fig 5, the switch is performs virtualization) includes stored virtual target descriptors (fig 12 see IP addresses) and stored physical target

descriptors (see figs 12 that show the address table contained within the switch shown in fig 5)

Latif makes no mention of buffering in the switch shown in fig 5 or the port shown in fig 15.

Latif does not specifically disclose at wire speed.

Ibrahim discloses at wire speed **(Col 4 lines 59-63 shows that the mappings of the virtual to the physical are performed, and data transfer is performed between the host and the storage device at wire speed, i.e. notice fig 3, where the elements within 302, have no need for a buffer, i.e. notice provisional application no. 60/317,817 page 9, 5.1.2, incorporated by reference, for showing mapping from virtual to physical at wirespeed and without buffering).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the switch apparatus of Latif, as taught by Ibrahim, since stated in Col 1 lines 60-65, that such a modification will overcome the effects of traffic on the network being slowed down and the overall throughput and latency deleteriously being reduced.

4. Claims 3-8, 10-16, 18, 24-29, 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Latif et al. (US 6400730) in view of Ibrahim (US 7330892) in view of Edsall et al. (US 6735198), hereinafter referred to as Edsall.

Regarding claim 3, Latif discloses utilizing the information **(Col 11 lines 50-55, where the destination IP address is equivalent to the address of a virtual target)**

about the virtual target **(Col 11 lines 50-55, where the destination IP address is equivalent to the address of a virtual target)** to update the packet **(Col 11 lines 15-30, where address translation from an IP address to a FC address is equivalent to an update)** with the second address **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target)** of the physical storage target **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target).**

The combined teachings of Latif and Ibrahim do not specifically disclose wherein the first port is located on a first line card and wherein the second port is located on a second line card, The first line card forwarding the packet to the second line card along with information about the virtual target.

Edsall discloses wherein the first port **(fig 5, see ports P0-P2 in LC 1)** is located on a first line card **(fig 5, see 1st line card LC1)** and wherein the second port **(fig 5, see ports P0-P2 of LC2)** is located on a second line card **(fig 5, LC 2 is equivalent to 2nd line card)**, The first line card **(fig 5, see 1st line card LC1)** forwarding the packet (fig 6 shows the fabric frame fwd from the ingress card to the egress card) to the second line card **(fig 5, LC 2 is equivalent to 2nd line card)** along with information about the virtual target **(fig 6, where a destination index or a VLAN ID is equivalent to virtual target info, i.e. the egress card uses this index to route data to the correct port according to Col 11 lines 22-32).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention was disclosed to modify the combined teachings of Latif and Ibrahim, as

taught by Edsall, since stated in Col 4 lines 1-12, that such a modification synchronizes forwarding tables, avoiding the problems that exist with the tables not having the same information.

Regarding claim 4, Latif discloses wherein the information about the virtual target is obtained from a virtual target descriptor **(Col 11 lines 50-55, where the destination IP address is equivalent to the address of a virtual target)**.

Regarding claim 5, Latif discloses wherein the information about the virtual target is obtained from a virtual target descriptor stored in a memory **(Col 11 lines 45-55, see conversion table equivalent to a memory).**

The combined teachings of Latif and Ibrahim do not specifically disclose on the first line card.

Edsall discloses on the first line card **(where fig 5 shows the forwarding tables, where information about a destination is obtained and inserted into a fabric frame in the ingress line card, such as the information that makes up the fabric frame in fig 6).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention was disclosed to modify the combined teachings of Latif and Ibrahim, as taught by Edsall, since stated in Col 4 lines 1-12, that such a modification synchronizes forwarding tables, avoiding the problems that exist with the tables not having the same information.

Regarding claim 6, Latif discloses utilizing information about the virtual target to obtain information about said physical target **(Col 11 lines 15-30, where address**

translation from an IP address to a FC address utilizes such information, and the conversion table assists in doing so).

The combined teaching of Latif and Ibrahim do not specifically disclose second line card.

Edsall discloses second line card **(fig 5, LC 2).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention was disclosed to modify the combined teachings of Latif and Ibrahim, as taught by Edsall, since stated in Col 4 lines 1-12, that such a modification synchronizes forwarding tables, avoiding the problems that exist with the tables not having the same information.

Regarding claim 7, Latif does not specifically disclose wherein the packet is for a particular request.

Ibrahim discloses wherein the packet is for a particular request (Col 4 lines 1-2, where the host requests for information/packets to be written).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the switch apparatus of Latif, as taught by Ibrahim, since stated in Col 1 lines 60-65, that such a modification will overcome the effects of traffic on the network being slowed down and the overall throughput and latency deleteriously being reduced.

The combined teaching of Latif and Ibrahim do not specifically disclose wherein at least one trace tag is associated with the packet and identifies information associated with the request.

Edsall discloses wherein at least one trace tag is associated with the packet and identifies information associated with the request (Col 4 lines 13-25, where the new address that is learned by each line card is equivalent to a trace tag).

It would have been obvious to one of the ordinary skill in the art at the time of the invention was disclosed to modify the combined teachings of Latif and Ibrahim, as taught by Edsall, since stated in Col 4 lines 1-12, that such a modification synchronizes forwarding tables, avoiding the problems that exist with the tables not having the same information.

Regarding claim 8, Latif discloses utilizing the information **(Col 11 lines 50-55, where the destination IP address is equivalent to the address of a virtual target)** about the virtual target **(Col 11 lines 50-55, where the destination IP address is equivalent to the address of a virtual target)** to update the packet **(Col 11 lines 15-30, where address translation from an IP address to a FC address is equivalent to an update)** with the second address **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target)** of the physical storage target **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target).**

The combined teachings of Latif and Ibrahim do not specifically disclose wherein the first port is located on a first line card and wherein the second port is located on a second line card, The first line card forwarding the packet to a plurality of line cards, including the second line card, along with information about the virtual target, wherein

each line card in the plurality of line cards includes a port in communication with a respective physical target device on which the virtual target is provisioned.

Edsall discloses wherein the first port **(fig 5, see ports P0-P2 in LC 1)** is located on a first line card **(fig 5, see 1st line card LC1)** and wherein the second port **(fig 5, see ports P0-P2 of LC2)** is located on a second line card **(fig 5, LC 2 is equivalent to 2nd line card)**, The first line card **(fig 5, see 1st line card LC1)** forwarding the packet to a plurality of line cards (Col 6 lines 10-25, floods the frame to other line cards) to the second line card **(fig 5, LC 2 is equivalent to 2nd line card)** along with information about the virtual target **(fig 6, where a destination index or a VLAN ID is equivalent to virtual target info, i.e. the egress card uses this index to route data to the correct port according to Col 11 lines 22-32),** wherein each line card (fig 5, see line cards) in the plurality of line cards includes a port **(fig 5, see ports P0-P2)** in communication with a respective physical target device **(fig 5, A, B and C are equivalent to target devices)** on which the virtual target is provisioned **(fig 6 shows a virtual address associated with a physical address, which proves provisioning).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention was disclosed to modify the combined teachings of Latif and Ibrahim, as taught by Edsall, since stated in Col 4 lines 1-12, that such a modification synchronizes forwarding tables, avoiding the problems that exist with the tables not having the same information.

Regarding claim 10, Latif discloses receiving at a first port **(fig 5, notice ports/interfaces in fig 5, where 270-5 includes an IP port interface)** of the switch **(fig**

5, notice switch fabric) a packet **(Col 2 lines 55-60 describes receiving a packet)** that specifies as a virtual storage target **(Col 11 lines 50-55, where the destination IP address is equivalent to the address of a virtual target)** provisioned on a physical storage target **(Col 11 lines 53-63, where the destination fibre channel address is equivalent to the address of the physical target, and is based/provisioned on the IP/virtual address, i.e. Col 5 lines 50-56, notice storage targets).**

utilizing the information **(Col 11 lines 50-55, where the destination IP address is equivalent to the address of a virtual target)** about the virtual target **(Col 11 lines 50-55, where the destination IP address is equivalent to the address of a virtual target)** to update the packet **(Col 11 lines 15-30, where address translation from an IP address to a FC address is equivalent to an update)** with the second address **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target)** of the physical storage target **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target).**

translating a first address **(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target)** of said virtual storage target **(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target)** to a second address **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target)** of said physical storage target (**Col 3 lines 1-5, packet is transmitted to a second network device coupled to the second port, i.e. Col 5 lines 50-56, notice storage targets)**

Latif makes no mention of buffering in the switch shown in fig 5 or the port shown in fig 15.

Latif does not specifically disclose without buffering.

Ibrahim discloses without buffering the packet **(Col 4 lines 59-63 shows that the mappings of the virtual to the physical are performed, and data transfer is performed between the host and the storage device at wire speed, i.e. notice fig 3, where the elements within 302, have no need for a buffer, i.e. notice provisional application no. 60/317,817 page 9, 5.1.2, incorporated by reference, for showing mapping from virtual to physical at wirespeed and without buffering).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the switch apparatus of Latif, as taught by Ibrahim, since stated in Col 1 lines 60-65, that such a modification will overcome the effects of traffic on the network being slowed down and the overall throughput and latency deleteriously being reduced.

The combined teachings of Latif and Ibrahim do not specifically disclose wherein the first port is located on a first line card and wherein the second port is located on a second line card, The first line card forwarding the packet to the second line card along with information about the virtual target. Sending by the second line card the packet to the physical storage target.

Edsall discloses wherein the first port **(fig 5, see ports P0-P2 in LC 1)** is located on a first line card **(fig 5, see 1st line card LC1)** and wherein the second port **(fig 5, see ports P0-P2 of LC2)** is located on a second line card **(fig 5, LC 2 is equivalent to 2nd**

line card), The first line card **(fig 5, see 1st line card LC1)** forwarding the packet (fig 6 shows the fabric frame fwd from the ingress card to the egress card) to the second line card **(fig 5, LC 2 is equivalent to 2nd line card)** along with information about the virtual target **(fig 6, where a destination index or a VLAN ID is equivalent to virtual target info, i.e. the egress card uses this index to route data to the correct port according to Col 11 lines 22-32).**

Sending by the second line card the packet to the physical storage target **(Col 11 lines 10-22, frame is transmitted to the egress line card that the station is attached to).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention was disclosed to modify the combined teachings of Latif and Ibrahim, as taught by Edsall, since stated in Col 4 lines 1-12, that such a modification synchronizes forwarding tables, avoiding the problems that exist with the tables not having the same information.

Regarding claim 11, Latif does not specifically disclose said virtualizing occurs at wire speed.

Ibrahim discloses said virtualizing occurs at wire speed **(Col 3 lines 15-20 shows wire speed, i.e. notice provisional application no. 60/317,817 page 9, 5.1.2, incorporated by reference, for showing mapping from virtual to physical at wirespeed and without buffering).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the switch apparatus of Latif, as taught by Ibrahim, since stated in

Col 1 lines 60-65, that such a modification will overcome the effects of traffic on the network being slowed down and the overall throughput and latency deleteriously being reduced.

Regarding claim 12, Latif discloses receiving at a first port **(fig 5, notice ports/interfaces in fig 5, where 270-5 includes an IP port interface)** of the switch **(fig 5, notice switch fabric)** a packet **(Col 2 lines 55-60 describes receiving a packet)** that specifies as a virtual storage target **(Col 11 lines 50-55, where the destination IP address is equivalent to the address of a virtual target)** provisioned on a physical storage target **(Col 11 lines 53-63, where the destination fibre channel address is equivalent to the address of the physical target, and is based/provisioned on the IP/virtual address, i.e. Col 5 lines 50-56, notice storage targets).**

utilizing the information **(Col 11 lines 50-55, where the destination IP address is equivalent to the address of a virtual target)** about the virtual target **(Col 11 lines 50-55, where the destination IP address is equivalent to the address of a virtual target)** to update the packet **(Col 11 lines 15-30, where address translation from an IP address to a FC address is equivalent to an update)** with the second address **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target)** of the physical storage target **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target).**

translating a first address **(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target)** of said virtual storage target

(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target) to a second address **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target)** of said physical storage target (**Col 3 lines 1-5, packet is transmitted to a second network device coupled to the second port, i.e. Col 5 lines 50-56, notice storage targets)**

Latif makes no mention of buffering in the switch shown in fig 5 or the port shown in fig 15.

Latif does not specifically disclose without buffering.

Ibrahim discloses without buffering the packet **(Col 4 lines 59-63 shows that the mappings of the virtual to the physical are performed, and data transfer is performed between the host and the storage device at wire speed, i.e. notice fig 3, where the elements within 302, have no need for a buffer, i.e. notice provisional application no. 60/317,817 page 9, 5.1.2, incorporated by reference, for showing mapping from virtual to physical at wirespeed and without buffering).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the switch apparatus of Latif, as taught by Ibrahim, since stated in Col 1 lines 60-65, that such a modification will overcome the effects of traffic on the network being slowed down and the overall throughput and latency deleteriously being reduced.

The combined teachings of Latif and Ibrahim do not specifically disclose wherein the first port is located on a first line card and wherein the second port is located on a second line card, The first line card forwarding the packet to a plurality of line cards,

including the second line card, along with information about the virtual target, wherein each line card in the plurality of line cards includes a port in communication with a respective physical target device on which the virtual target is provisioned.

Edsall discloses wherein the first port **(fig 5, see ports P0-P2 in LC 1)** is located on a first line card **(fig 5, see 1st line card LC1)** and wherein the second port **(fig 5, see ports P0-P2 of LC2)** is located on a second line card **(fig 5, LC 2 is equivalent to 2nd line card)**, The first line card **(fig 5, see 1st line card LC1)** forwarding the packet to a plurality of line cards (Col 6 lines 10-25, floods the frame to other line cards) to the second line card **(fig 5, LC 2 is equivalent to 2nd line card)** along with information about the virtual target **(fig 6, where a destination index or a VLAN ID is equivalent to virtual target info, i.e. the egress card uses this index to route data to the correct port according to Col 11 lines 22-32),** wherein each line card (fig 5, see line cards) in the plurality of line cards includes a port **(fig 5, see ports P0-P2)** in communication with a respective physical target device **(fig 5, A, B and C are equivalent to target devices)** on which the virtual target is provisioned **(fig 6 shows a virtual address associated with a physical address, which proves provisioning).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention was disclosed to modify the combined teachings of Latif and Ibrahim, as taught by Edsall, since stated in Col 4 lines 1-12, that such a modification synchronizes forwarding tables, avoiding the problems that exist with the tables not having the same information.

Regarding claim 13, Latif does not specifically disclose said virtualizing occurs at wire speed.

Ibrahim discloses said virtualizing occurs at wire speed **(Col 3 lines 15-20 shows wire speed, i.e. notice provisional application no. 60/317,817 page 9, 5.1.2, incorporated by reference, for showing mapping from virtual to physical at wirespeed and without buffering).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the switch apparatus of Latif, as taught by Ibrahim, since stated in Col 1 lines 60-65, that such a modification will overcome the effects of traffic on the network being slowed down and the overall throughput and latency deleteriously being reduced.

Regarding claim 14, Latif discloses receiving at a first port **(fig 5, notice ports/interfaces in fig 5, where 270-5 includes an IP port interface)** of the switch **(fig 5, notice switch fabric)** a packet **(Col 2 lines 55-60 describes receiving a packet)** that specifies as a virtual storage target **(Col 11 lines 50-55, where the destination IP address is equivalent to the address of a virtual target)** provisioned on a physical storage target **(Col 11 lines 53-63, where the destination fibre channel address is equivalent to the address of the physical target, and is based/provisioned on the IP/virtual address, i.e. Col 5 lines 50-56, notice storage targets).**

Using the information **(Col 11 lines 50-55, where the destination IP address is equivalent to the address of a virtual target)** about the virtual target **(Col 11 lines 50-55, where the destination IP address is equivalent to the address of a virtual**

target) to update the packet **(Col 11 lines 15-30, where address translation from an IP address to a FC address is equivalent to an update)** with the second address **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target)** of the physical storage target **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target).**

Converting a first address **(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target)** of said virtual storage target **(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target)** to a second address **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target)** of said physical storage target (**Col 3 lines 1-5, packet is transmitted to a second network device coupled to the second port, i.e. Col 5 lines 50-56, notice storage targets)**

Latif makes no mention of buffering in the switch shown in fig 5 or the port shown in fig 15.

Latif does not specifically disclose without buffering.

Ibrahim discloses without buffering the packet **(Col 4 lines 59-63 shows that the mappings of the virtual to the physical are performed, and data transfer is performed between the host and the storage device at wire speed, i.e. notice fig 3, where the elements within 302, have no need for a buffer, i.e. notice provisional application no. 60/317,817 page 9, 5.1.2, incorporated by reference, for showing mapping from virtual to physical at wirespeed and without buffering).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the switch apparatus of Latif, as taught by Ibrahim, since stated in Col 1 lines 60-65, that such a modification will overcome the effects of traffic on the network being slowed down and the overall throughput and latency deleteriously being reduced.

The combined teachings of Latif and Ibrahim do not specifically disclose an ingress line card, the information including a flowID for routing the packet through the switch, and the ingress line card placing a virtual target descriptor identifier and the flow ID, in a local header of the packet, the ingress line card forwarding the packet to a fabric, which forwards the packet to an egress line card in accordance with the flow ID, And an egress line card.

Edsall discloses an ingress line card (fig 5, see line cards, where the source line card is equivalent to an ingress), the information including a flowID (fig 6, see POE bit vector) for routing the packet through the switch (Col 9 lines 49-51, instructing the switch fabric as to which line card), and the ingress line card (fig 5, LC 1, line card 1 equivalent to ingress line card) placing a virtual target descriptor identifier (fig 6, VLAN ID or dest index is equivalent to virtual descriptor) and the flow ID (fig 6, see POE bit vector), in a local header of the packet (fig 6, fabric header), the ingress line card (fig 5, LC 1, line card 1 equivalent to ingress line card) forwarding the packet to a fabric (fig 6, LC 1 fwds packet to switch fabric 550), which forwards the packet to an egress line card (fig 5, dest line card such as LC 2 is equivalent to egress) in accordance with the flow ID (Col 9 lines 49-51, POE bit vector instructing the switch fabric as to which line card),

It would have been obvious to one of the ordinary skill in the art at the time of the invention was disclosed to modify the combined teachings of Latif and Ibrahim, as taught by Edsall, since stated in Col 4 lines 1-12, that such a modification synchronizes forwarding tables, avoiding the problems that exist with the tables not having the same information.

Regarding claim 15, Latif does not specifically disclose wherein the packet is for a particular request.

Ibrahim discloses wherein the packet is for a particular request (Col 4 lines 1-2, where the host requests for information/packets to be written).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the switch apparatus of Latif, as taught by Ibrahim, since stated in Col 1 lines 60-65, that such a modification will overcome the effects of traffic on the network being slowed down and the overall throughput and latency deleteriously being reduced.

The combined teaching of Latif and Ibrahim do not specifically disclose wherein at least one trace tag is associated with the packet and identifies information associated with the request, the egress line card including the trace tag as a source identifier with the packet sent.

Edsall discloses wherein at least one trace tag is associated with the packet and identifies information associated with the request (Col 4 lines 13-25, where the new address that is learned by each line card is equivalent to a trace tag), the egress line

card including the trace tag as a source identifier with the packet sent (Col 6 lines 40-5, where each forwards engine of the flooded line cards learn the source address).

It would have been obvious to one of the ordinary skill in the art at the time of the invention was disclosed to modify the combined teachings of Latif and Ibrahim, as taught by Edsall, since stated in Col 4 lines 1-12, that such a modification synchronizes forwarding tables, avoiding the problems that exist with the tables not having the same information.

<u>Regarding claim 16,</u> Latif does not specifically disclose said virtualizing occurs at wire speed.

Ibrahim discloses said virtualizing occurs at wire speed **(Col 3 lines 15-20 shows wire speed, i.e. notice provisional application no. 60/317,817 page 9, 5.1.2, incorporated by reference, for showing mapping from virtual to physical at wirespeed and without buffering).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the switch apparatus of Latif, as taught by Ibrahim, since stated in Col 1 lines 60-65, that such a modification will overcome the effects of traffic on the network being slowed down and the overall throughput and latency deleteriously being reduced.

<u>Regarding claim 18,</u> Latif discloses a table for storing translation information including identifiers, where one skilled in the art interprets a table as memory such as a CAM or SRAM.

Furthermore, the line cards of Edsall teach forwarding tables (see fig 5), where such tables are interpreted as memories such as CAM's or SRAM's.

Regarding claim 24, Latif discloses receiving at a first port **(fig 5, notice ports/interfaces in fig 5, where 270-5 includes an IP port interface)** of the switch **(fig 5, notice switch fabric)** a packet **(Col 2 lines 55-60 describes receiving a packet)**

A processor unit associated with and in communication with the port **(figs 15 and 16, see routing logic).**

translating a first address **(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target)** of said virtual storage target **(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target)** provisioned on a physical storage target **(Col 11 lines 53-63, where the destination fibre channel address is equivalent to the address of the physical target, and is based/provisioned on the IP/virtual address, i.e. Col 5 lines 50-56, notice storage targets)** to a second address **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target)** of said physical storage target (**Col 3 lines 1-5, packet is transmitted to a second network device coupled to the second port, i.e. Col 5 lines 50-56, notice storage targets)**

Latif does not specifically disclose without buffering.

Ibrahim discloses without buffering the packet **(Col 4 lines 59-63 shows that the mappings of the virtual to the physical are performed, and data transfer is performed between the host and the storage device at wire speed, i.e. notice fig 3,**

where the elements within 302, have no need for a buffer, i.e. notice provisional application no. 60/317,817 page 9, 5.1.2, incorporated by reference, for showing mapping from virtual to physical at wirespeed and without buffering).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the switch apparatus of Latif, as taught by Ibrahim, since stated in Col 1 lines 60-65, that such a modification will overcome the effects of traffic on the network being slowed down and the overall throughput and latency deleteriously being reduced.

The combined teachings of Latif and Ibrahim do not specifically disclose a plurality of line cards and wherein the switch further comprises a CPU in communication with the processor unit, the CPU sending the processor unit a virtual target descriptor with information for the processor unit to operate on data for said virtual storage target.

Esdall discloses a plurality of line cards (see fig 5 plurality of LC's).

wherein the switch further comprises a CPU (fig 5, where the combination of the EARL and LTL are equivalent to CPU) in communication with the processor unit (fig 5, the port is equivalent to a processor unit), the CPU sending the processor unit a virtual target descriptor (fig 6, where the port circuitry appends a header including dest index and VLAN ID in the line card) with information for the processor unit to operate on data for said virtual storage target (the operation of appending the fabric header with information).

It would have been obvious to one of the ordinary skill in the art at the time of the invention was disclosed to modify the combined teachings of Latif and Ibrahim, as

taught by Edsall, since stated in Col 4 lines 1-12, that such a modification synchronizes forwarding tables, avoiding the problems that exist with the tables not having the same information.

<u>Regarding claim 25,</u> Latif does not specifically disclose said virtualizing occurs at wire speed.

Ibrahim discloses said virtualizing occurs at wire speed **(Col 3 lines 15-20 shows wire speed, i.e. notice provisional application no. 60/317,817 page 9, 5.1.2, incorporated by reference, for showing mapping from virtual to physical at wirespeed and without buffering).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the switch apparatus of Latif, as taught by Ibrahim, since stated in Col 1 lines 60-65, that such a modification will overcome the effects of traffic on the network being slowed down and the overall throughput and latency deleteriously being reduced.

<u>Regarding claim 26,</u> The combined teachings of Latif and Ibrahim do not specifically disclose wherein each line card includes a plurality of ports and a plurality of processor units, wherein each processor unit is in communication with at least one respective port.

Edsall discloses wherein each line card includes a plurality of ports and a plurality of processor units, wherein each processor unit is in communication with at least one respective port (see fig 5, where each line card contains a number of components).

It would have been obvious to one of the ordinary skill in the art at the time of the invention was disclosed to modify the combined teachings of Latif and Ibrahim, as taught by Edsall, since stated in Col 4 lines 1-12, that such a modification synchronizes forwarding tables, avoiding the problems that exist with the tables not having the same information.

Regarding claim 27, The combined teachings of Latif and Ibrahim do not specifically disclose the processor unit including a PACE and a PPU.

Edsall discloses a PACE (fig 5, LTL) and a PPU (UDLINK).

It would have been obvious to one of the ordinary skill in the art at the time of the invention was disclosed to modify the combined teachings of Latif and Ibrahim, as taught by Edsall, since stated in Col 4 lines 1-12, that such a modification synchronizes forwarding tables, avoiding the problems that exist with the tables not having the same information.

Regarding claim 28, Latif discloses a table for storing translation information including identifiers, where one skilled in the art interprets a table as memory such as a CAM or SRAM.

Furthermore, the line cards of Edsall teach forwarding tables (see fig 5), where such tables are interpreted as memories such as CAM's or SRAM's.

Regarding claim 29, Latif discloses receiving at a first port **(fig 5, notice ports/interfaces in fig 5, where 270-5 includes an IP port interface)** of the switch **(fig 5, notice switch fabric)** a packet **(Col 2 lines 55-60 describes receiving a packet)**

A processor unit (fig 15 each port contains a number of processors) coupled to a traffic manager (fig 5, 250 shows management processor), which is coupled to a fabric (fig 5, 240 shows fabric) for routing packets from an ingress (fig 5, 250 is ingress) to an egress **(fig 5, see ports and interfaces for egress).**

translating a first address **(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target)** of said virtual storage target **(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target)** provisioned on a physical storage target **(Col 11 lines 53-63, where the destination fibre channel address is equivalent to the address of the physical target, and is based/provisioned on the IP/virtual address, i.e. Col 5 lines 50-56, notice storage targets)** to a second address **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target)** of said physical storage target (**Col 3 lines 1-5, packet is transmitted to a second network device coupled to the second port, i.e. Col 5 lines 50-56, notice storage targets)**

each port is associated with a respective processor unit (fig 15 and 16 show routing logic/processor) which is coupled to a management processor (traffic manager) such as fig 5 250.

Latif does not specifically disclose at wire speed.

Ibrahim discloses at wire speed **(Col 4 lines 59-63 shows that the mappings of the virtual to the physical are performed, and data transfer is performed between the host and the storage device at wire speed, i.e. notice fig 3, where the elements**

within 302, have no need for a buffer, i.e. notice provisional application no. 60/317,817 page 9, 5.1.2, incorporated by reference, for showing mapping from virtual to physical at wirespeed and without buffering).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the switch apparatus of Latif, as taught by Ibrahim, since stated in Col 1 lines 60-65, that such a modification will overcome the effects of traffic on the network being slowed down and the overall throughput and latency deleteriously being reduced.

The combined teaching of Latif and Ibrahim do not specifically disclose a plurality of line cards.

Edsall discloses a plurality of line cards (see fig 5, LC's).

It would have been obvious to one of the ordinary skill in the art at the time of the invention was disclosed to modify the combined teachings of Latif and Ibrahim, as taught by Edsall, since stated in Col 4 lines 1-12, that such a modification synchronizes forwarding tables, avoiding the problems that exist with the tables not having the same information.

<u>Regarding claim 32,</u> Latif discloses a plurality of ports **(fig 5, notice ports/interfaces in fig 5, where 270-5 includes an IP port interface)**

Wherein said sending comprises virtualizing said packet **(Col 11 lines 15-30, where address translation from an IP address to a FC address is equivalent to virtualizing)** by translating a first address **(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target)** of said virtual storage target

(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target) to a second address **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target)** of said physical storage target (**Col 3 lines 1-5, packet is transmitted to a second network device coupled to the second port, i.e. Col 5 lines 50-56, notice storage targets)**

Latif makes no mention of buffering in the switch shown in fig 5 or the port shown in fig 15.

Latif does not specifically disclose at wire speed.

Ibrahim discloses at wire speed **(Col 4 lines 59-63 shows that the mappings of the virtual to the physical are performed, and data transfer is performed between the host and the storage device at wire speed, i.e. notice fig 3, where the elements within 302, have no need for a buffer, i.e. notice provisional application no. 60/317,817 page 9, 5.1.2, incorporated by reference, for showing mapping from virtual to physical at wirespeed and without buffering).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the switch apparatus of Latif, as taught by Ibrahim, since stated in Col 1 lines 60-65, that such a modification will overcome the effects of traffic on the network being slowed down and the overall throughput and latency deleteriously being reduced.

The combined teaching of Latif and Ibrahim do not specifically disclose a plurality of line cards.

Edsall discloses a plurality of line cards (see fig 5, LC's).

It would have been obvious to one of the ordinary skill in the art at the time of the invention was disclosed to modify the combined teachings of Latif and Ibrahim, as taught by Edsall, since stated in Col 4 lines 1-12, that such a modification synchronizes forwarding tables, avoiding the problems that exist with the tables not having the same information.

Regarding claim 33, Latif does not specifically disclose said virtualizing occurs at wire speed.

Ibrahim discloses said virtualizing occurs at wire speed **(Col 3 lines 15-20 shows wire speed, i.e. notice provisional application no. 60/317,817 page 9, 5.1.2, incorporated by reference, for showing mapping from virtual to physical at wirespeed and without buffering).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the switch apparatus of Latif, as taught by Ibrahim, since stated in Col 1 lines 60-65, that such a modification will overcome the effects of traffic on the network being slowed down and the overall throughput and latency deleteriously being reduced.

Regarding claim 34, Latif discloses receiving at a first port **(fig 5, notice ports/interfaces in fig 5, where 270-5 includes an IP port interface)** of the switch **(fig 5, notice switch fabric)** a packet **(Col 2 lines 55-60 describes receiving a packet)** that specifies as a virtual storage target **(Col 11 lines 50-55, where the destination IP address is equivalent to the address of a virtual target)** provisioned on a physical storage target **(Col 11 lines 53-63, where the destination fibre channel address is**

equivalent to the address of the physical target, and is based/provisioned on the IP/virtual address, i.e. Col 5 lines 50-56, notice storage targets).

utilizing the information **(Col 11 lines 50-55, where the destination IP address is equivalent to the address of a virtual target)** about the virtual target **(Col 11 lines 50-55, where the destination IP address is equivalent to the address of a virtual target)** to update the packet **(Col 11 lines 15-30, where address translation from an IP address to a FC address is equivalent to an update)** with the second address **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target)** of the physical storage target **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target).**

translating a first address **(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target)** of said virtual storage target **(Col 11 lines 15-30, where an IP address is equivalent to a first address of a virtual storage target)** to a second address **(Col 11 lines 15-30, where the FC address is equivalent to a second address and is the address of the physical target)** of said physical storage target (**Col 3 lines 1-5, packet is transmitted to a second network device coupled to the second port, i.e. Col 5 lines 50-56, notice storage targets)**

Latif makes no mention of buffering in the switch shown in fig 5 or the port shown in fig 15.

Latif does not specifically disclose without buffering.

Ibrahim discloses without buffering the packet **(Col 4 lines 59-63 shows that the mappings of the virtual to the physical are performed, and data transfer is performed between the host and the storage device at wire speed, i.e. notice fig 3, where the elements within 302, have no need for a buffer, i.e. notice provisional application no. 60/317,817 page 9, 5.1.2, incorporated by reference, for showing mapping from virtual to physical at wirespeed and without buffering).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the switch apparatus of Latif, as taught by Ibrahim, since stated in Col 1 lines 60-65, that such a modification will overcome the effects of traffic on the network being slowed down and the overall throughput and latency deleteriously being reduced.

The combined teachings of Latif and Ibrahim do not specifically disclose wherein the first port is located on a first line card and wherein the second port is located on a second line card, The first line card forwarding the packet to a plurality of line cards, including the second line card, along with information about the virtual target, wherein each line card in the plurality of line cards includes a port in communication with a respective physical target device on which the virtual target is provisioned.

Edsall discloses wherein the first port **(fig 5, see ports P0-P2 in LC 1)** is located on a first line card **(fig 5, see 1st line card LC1)** and wherein the second port **(fig 5, see ports P0-P2 of LC2)** is located on a second line card **(fig 5, LC 2 is equivalent to 2nd line card)**, The first line card **(fig 5, see 1st line card LC1)** forwarding the packet to a plurality of line cards (Col 6 lines 10-25, floods the frame to other line cards) to the

second line card **(fig 5, LC 2 is equivalent to 2nd line card)** along with information about the virtual target **(fig 6, where a destination index or a VLAN ID is equivalent to virtual target info, i.e. the egress card uses this index to route data to the correct port according to Col 11 lines 22-32),** wherein each line card (fig 5, see line cards) in the plurality of line cards includes a port **(fig 5, see ports P0-P2)** in communication with a respective physical target device **(fig 5, A, B and C are equivalent to target devices)** on which the virtual target is provisioned **(fig 6 shows a virtual address associated with a physical address, which proves provisioning).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention was disclosed to modify the combined teachings of Latif and Ibrahim, as taught by Edsall, since stated in Col 4 lines 1-12, that such a modification synchronizes forwarding tables, avoiding the problems that exist with the tables not having the same information.

Regarding claim 35, Latif does not specifically disclose said virtualizing occurs at wire speed.

Ibrahim discloses said virtualizing occurs at wire speed **(Col 3 lines 15-20 shows wire speed, i.e. notice provisional application no. 60/317,817 page 9, 5.1.2, incorporated by reference, for showing mapping from virtual to physical at wirespeed and without buffering).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the switch apparatus of Latif, as taught by Ibrahim, since stated in Col 1 lines 60-65, that such a modification will overcome the effects of traffic on the

network being slowed down and the overall throughput and latency deleteriously being reduced.

Allowable Subject Matter

5. Claims 19-23 are allowed (maintained from previous office action).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Shanbhag et al. (US 20050198523) teaches address mapping between virtual and physical addresses being performed at wire speed.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER P. GREY whose telephone number is (571)272-3160. The examiner can normally be reached on 10AM-7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Moe Aung can be reached on (571)272-7314. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aung S. Moe/
Supervisory Patent Examiner, Art Unit 2474

/Christopher P Grey/
Examiner, Art Unit 2474